REMARKS

This Amendment and Response is filed in reply to the Office action dated April 27, 2007. Claims 83-102 are amended and claims 2, 26, 52, 65 and 70 were previously canceled. Accordingly, after entry of this Amendment and Response, claims 1, 3-25, 27-51, 53-64, 66-69 and 71-102 remain pending.

I. Claim Rejections Under 35 U.S.C. § 112

Claims 1, 3-25, 27-51, 53-64, 66-69 and 71-102 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. More specifically, the original specification does not have support for the added limitation in each of the independent claims 1, 25, 38, 50, 64, 68, 83 and 99. For example, in claim 1, the Office action alleges that the added limitation of "while ignoring those instances of read operations unavailable in the low-latency memory requested from a second low-latency memory" is new matter. The Applicant respectfully submits that the previously submitted amendments have proper support in the specification and are not new matter for at least the following reasons.

Under 35 U.S.C. § 112, first paragraph, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. As such, there is no *in haec verba* requirement for claim amendments (i.e., the newly added claim limitation does not have to use the exact language in the specification). *See MPEP* § 2163.I.B.

In the specification, a low latency memory is described as memory that operates at a speed at least sufficient to avoid stalling an accessing processing unit. *See Specification*, paragraph 1021. Examples of low latency memory are L1 and L2 caches. *See Id.* Conversely, high latency memory, including L3 caches and main memory, is memory that operates at a speed insufficient to avoid stalling an accessing processing unit. *See Id.* The performance of an accessing processing unit decreases when it stalls on a memory access such as a read operation.

Further, the specification, referring to Figure 1, indicates that the memory operations module 101 requests respective values for the read operations instances 103, 105, and 107 from a low-latency memory (e.g., L1 cache, L2 cache, etc.). *See Specification*, paragraph 1023. These values are supplied from the low-latency memory 111 to the memory operations module for the read operations instances 103 and 105 (i.e., they hit in the low-latency memory). *See Id.* However, the value(s) for the read operation instance 107 misses in the low-latency memory and is not supplied. *See Id.* In such instances, the memory operations unit queries the missing read operation value predictor for the read operation instance 107 and queries a high-latency memory (e.g., off-chip cache, main memory, etc.)

for the value(s). *See Specification*, paragraph 1024. When the value predictor returns a value, the read operation is speculatively executed with the returned value; otherwise the processing unit stalls until a value is returned from the high latency memory. *See Id.* Thus, performance can be improved by value predicting misses in high latency memory. The size of the value prediction structure is minimized by not value predicting misses in low latency memory.

The original independent claims included a limitation of the processor value predicting for those instances of read operations with values that are unavailable in a low-latency memory and requested from a high-latency memory. Given that low-latency memory may be L1 and/or L2 caches, the Applicant respectfully submits that values that are unavailable in a low-latency memory may be from either a L1 or L2 cache. Only when an unavailable value is fetched from a high-latency cache is value prediction performed. Therefore, the limitation "while ignoring those instances of read operations unavailable in the low-latency memory requested from a second low-latency memory" is clearly supported, both explicitly and implicitly, in the specification and is not new matter. Therefore, the Applicant, respectfully submits that the independent claims 1, 25, 38, 50, 64, 68, 83 and 99 comply with 35 U.S.C. § 112, first paragraph, are in form for allowance, and such indication is respectfully requested.

II. Claim Rejections Under 35 U.S.C. § 101

Claims 83-102 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Specifically, the computer readable medium of claims 83-102 cover embodiments where the medium is a signal per se. In response, claims 83-102 have been amended to each recite an article of manufacture, a tangible product. It is respectfully submitted that claims 83-102, as amended, are in compliance with 35 U.S.C. § 101 and such indication is respectfully requested.

III. Conclusion

The Applicant thanks the Examiner for his thorough review of the application. The Applicant respectfully submits the present application, as amended, is in condition for allowance and respectfully requests the issuance of a Notice of Allowability as soon as practicable.

The Applicant believes no fees or petitions are due with this filing. However, should any such fees or petitions be required, please consider this a request therefor and authorization to charge Deposit Account No. 04-1415 as necessary.

If the Examiner should require any additional information or amendment, please contact the undersigned attorney.

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Respectfully submitted,

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